REMARKS

Applicants respectfully request reconsideration of the present application in view of the reasons that follow.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

No claims have been amended. Claims 1-31 remain pending in this application, of which claims 25-31 are withdrawn from consideration.

Allowable subject matter

Applicants appreciate the indication that claims 14-24 are allowed and claims 2-3, 5-6 and 8-9 contain allowable subject matter.

Rejection under 35 U.S.C. § 102

Claims 1, 4, 7 and 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,760,644 to Lancaster et al. ("Lancaster"). Applicants respectfully traverse this rejection for at least the following reasons.

Independent claim 1 is directed to a time limit function utilization apparatus, and comprises a semiconductor time switch which is interposed in or connected to a signal line (which connects a first functional block and a second functional block), and substantially disables or substantially enables mutual access between the first functional block and second functional block upon a lapse of a first predetermined time. Lancaster fails to disclose or suggest a semiconductor time switch interposed in or connected to a signal line, which connects a first functional block and a second functional block, where the time switch disables or substantially enables mutual access between the first functional block and second functional block upon a lapse of time.

The Office Action equates a power supply and memory of Lancaster with the first and second functional blocks, respectively, as recited in claim 1, citing to Lancaster at column 2,

lines 25 – 28, and further cites to Lancaster in the abstract and Figures 2-5 as disclosing the semiconductor time switch as recited. Lancaster, however, merely discloses in col. 2, lines 25-28 that its timer/clock may be used to trigger the refresh operation of a memory whenever power is available. Significantly, Lancaster does not disclose that his timer substantially disables or substantially enables mutual access between the power supply or memory, even if the power supply and memory could be considered to be functional blocks. FIGS. 3 and 5 of Lancaster merely show that the timer of FIG. 1 can utilize charging/discharging of SONOS in its functioning. None of these figures suggests the time limit function utilization apparatus of claim 1, which connects or disconnects mutual access between first and second functional blocks.

Applicants note that the time switch as recited in claim 1, does not merely act as a timer, but is arranged relative to two functional blocks, such as a memory and a decoder as shown in FIG. 1 for example, and thereby connects or disconnects the signal line provided therebetween after a predetermined time period. By contrast, the Lancaster timer is not arranged as a bridge between two functional blocks, and thus Lancaster does not anticipate the time limit function utilization apparatus as in claim 1.

Lancaster does not disclose that its timer connects or disconnects mutual access between two functional blocks. Lancaster discloses that its timing device is preferably a FET called SONOS or SNOS. FIGS. 2 - 5 of Lancaster merely show a structure of SONOS or SNOS and the voltage characteristics thereof. In the structure of SONOS, for example, positively charged holes trapped in nitride layer 20' in FIG. 3 are released over a period of time, resulting in a change in threshold value as indicated in, for example, FIG. 4. The change in threshold value is used in the timer function of the Lancaster timer. Lancaster, however, merely discloses replaceably reading a voltage change between two conductors as a time change as shown in FIG. 2. Lancaster does not disclose any time limit function utilization apparatus which connects or disconnects the mutual access between two functional blocks.

The Office Action also states that Lancaster discloses and shows a signal line in column 2, lines 20 - 25 and the front page diagram. The front page diagram of Lancaster, however, merely shows a circuit which measures the voltage between conductors 1 and 2 in timer 30 using voltage measurement circuit 100. If the Examiner maintains the rejection based on Lancaster, applicants respectfully request that the Examiner specifically point out the location of a signal line in Lancaster that connects two functional blocks.

The claims ultimately depending from claim 1 are patentable for at least the same reasons, as well as for further patentable features recited therein. For example, Lancaster does not disclose all the features of dependent claim 7. The Office Action appears to equate elements 301 and 302 of Lancaster with the "other terminal" of claim 7, which is connected to the third functional block, and the first input/ouput terminal, respectively. In claim 7, the third functional block is arranged such that it may have access to the first functional block after the time limit of the time switch. By contrast, the electrode 301 of Lancaster is a gate electrode of a SONOS device, and is not able to have access to electrode 302 or 303 regardless of the time limit of the time switch. Thus, Lancaster does not disclose the arrangement of the three functional blocks relative to the terminals in the manner recited in claim 7.

Dependent claim 11 recites "by supplying charges to the gate electrode in advance." By contrast, Lancaster discloses only storing charge in nitride 32', not in a gate electrode, which would correspond to the poly gate of Lancaster. Generally nitride stores charge in local traps within the nitride. The nitride, however, would not be considered a gate electrode because it is not a conductor where electric current flows inside. Thus, Lancaster does not suggest the features of claim 11.

Dependent claim 12 recites the charges are injected into or leak from a gate electrode via a semiconductor or Schottky junction. By contrast, in FIG. 3 of Lancaster, charges leaking from a memory nitride come through oxide layer 42, not through N/P/N junctions (50/60/50).

Dependent claim 13 recites the charges are injected into or leak from a gate electrode via an insulating member. By contrast, Lancaster discloses that it is not the gate electrode, but local traps 32 in the memory nitride that store the charges.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date November 30, 2005 By _____

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 672-5414
Facsimile: (202) 672-5399

Richard L. Schwaab
Attorney for Applicant
Registration No. 25,479

Thomas G. Bilodeau
Attorney for Applicant
Registration No. 43,438